Selective Deposition of High-k Capping Layer on MoS_2 Field Effect Transistors by Using Graphene Electrodes

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Abstract

It is demonstrated that capping high-k layer on MoS_2 FETs can strongly dampen the Coulombic scattering of charge carriers due to the dielectric constant mismatch between nanoscale channel material and the high-k dielectric[1]. Meanwhile, high-k materials deposited by Atomic Layer Deposition (ALD) exhibit the best electronic properties. However, the photoresist used in lithography process could seriously contaminate the MoS_2 channel during the patterning of high-k material. Moreover, it is also impossible to use common shadow mask to prevent high-k material from depositing on the metallic electrodes in the ALD process owing to its growing mechanism. In this work, we demonstrated a new method in which graphene was chosen as the electrode material, where ALD materials were difficult to deposit on top.

Figure 1 illustrates the schematic flow of the fabrication process of our devices. Few-layer MoS_2 flakes were mechanically exfoliated by the classical scotch-tape technique and transferred to a heavily doped silicon substrate capped with 300 nm SiO_2. We used the heavily doped silicon substrate as the bottom gate.The best candidate of flakes was chosen by optical microscopy (**Fig. 2a**) and its thickness was checked by AFM (**Fig. 2b**). A layer thickness in the range of 6−12 nm would be ideal.[2] Then, two few-layer graphene flakes serving as source and drain were transferred to the target position on top of the MoS_2 by PDMS stamping, which is an all-dry method.[3] After the transfer process, two-step annealing was conducted. First, the devices were annealed at 200°C in an Ar atmosphere for 2h (100 sccm) to remove residue. Secondly, the devices were annealed at 120 °C for up to 20 h in high vacuum ($\sim10^{-7}$ torr) before measurement. It is believed that in situ vacuum annealing can dope devices and significantly reduce Schottky barrier height and contact resistance[4]. High-k materials are difficult to deposit on pristine graphene by ALD because of its perfect symmetry and strong global π bond.[5,6] On the contrary, there is a small window to deposit high-k material on $MoS_2$by ALD if we select appropriate growth temperature, purge time, and pause time.[6] Therefore, a 20 nm ALD-Al_2O_3 layer was deposited on MoS_2 surface at 200 °C without any resist. The graphene electrodes wouldn't be capped by Al_2O_3 thanks to its selectivity.

The transfer (I_d-V_g) and output I-V characteristics (I_d-V_d) of the device are shown in **Fig.3**. It is fairly clear that the graphene is not capped by Al_2O_3. The device shows n-type conduction. The field effect mobility and I_{on}/I_{off} of the device before ALD deposition are about 1.81 $cm^2\ V^{-1}s^{-1}$ and $10^{3.5}$(**Fig. 3a**), respectively. After Al_2O_3 deposition, the field effect mobility and I_{on}/I_{off} of the device are enhanced to 13 $cm^2\ V^{-1}s^{-1}$ and 10^5. (**Fig. 3b**) Thissignificant enhancement of device performance can be attributed to the dielectric engineering of Al_2O_3, which helps screening the Coulombic scattering of carriers. Also, the optimized thickness helps striking the balance between Thomas-Fermi charge screening and interlayer coupling according to the resist network model[7],so that this mobility value is three times higher than the MoS_2 FETs with graphene electrodes in previous literature.[8] In addition, the output I-V characteristics (**Fig. 3**d) display linear and saturation regions in low and high V_d ranges, respectively. The linear part is attributed to the quasi-ohmic contact between MoS_2 and graphene, while the saturation arises from the channel pinch-off.

In conclusion, MoS_2 FETs using graphene as electrodes shows excellent electronic properties: current on/off ratio ($\sim10^5$) and a field effect mobility of $\sim$13 $cm^2\ V^{-1}\ s^{-1}$. ALD-$Al_2O_{3\ capping}$ can not only enhance the mobility but offer relatively dense passivation. Besides, water molecules adsorbed on the surface of MoS_2 before passivation can be removed since water is the precursor in the growth process of ALD. More importantly, with graphene as the electrodes, the selective growth of ALD-Al_2O_3 between MoS_2 and graphene provides a resist-free passivation process, which can eliminate the possibility of contamination from resist.

References

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Figures

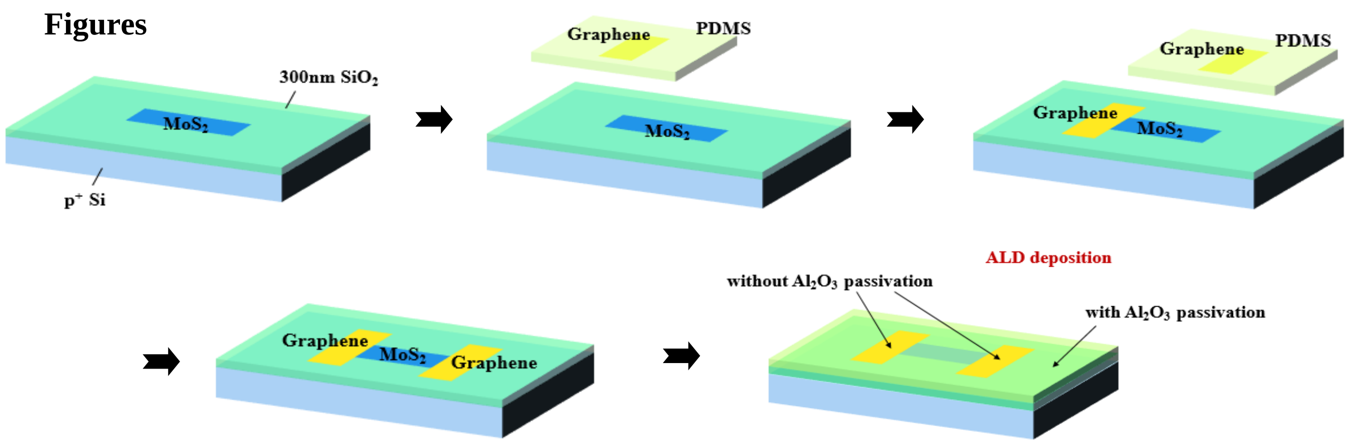

Fig. 1 Schematic fabrication process of MoS_2 FET with graphene electrode.

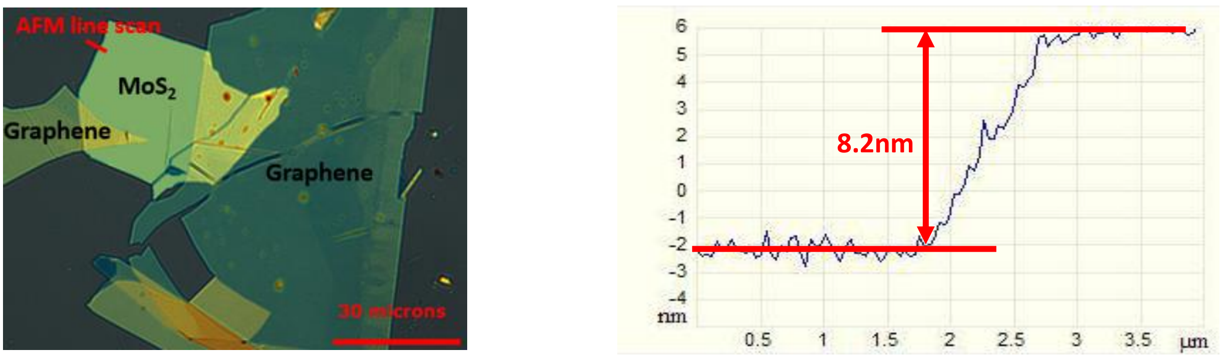

Fig. 2 (a) The OM image of MoS_2 FET device. **(b)** AFM line profile of MoS_2

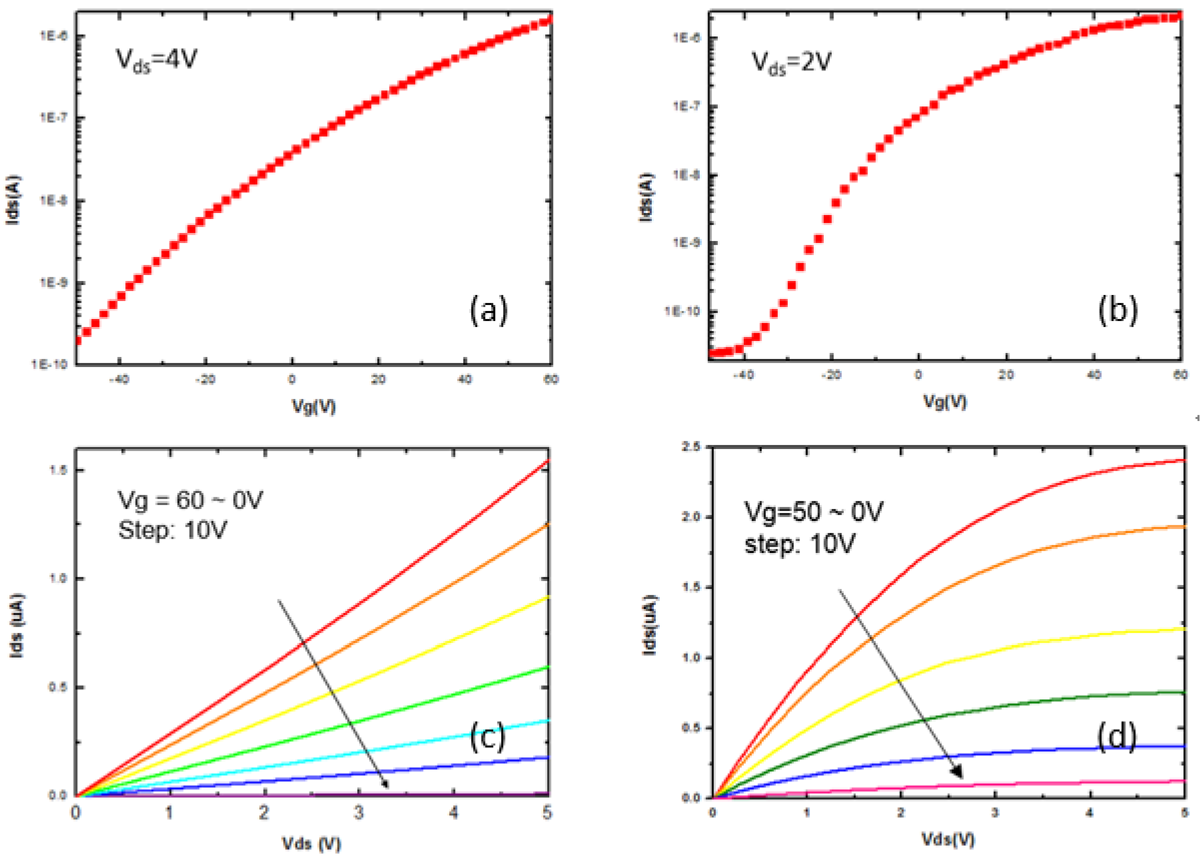

Fig. 3 (a)(c) Transfer and Output characteristics of MoS_2 FET before ALD deposition
(b)(d) Transfer and Output characteristics of MoS_2 FET after ALD deposition